REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R008-92.	91-10-18	M. A. Frye
B	Changes in footnotes at end of table I. Editorial changes throughout.	92-10-29	M. A. Frye
C	Update drawing to current requirements. Editorial changes throughout. – drw	04-09-14	Raymond Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
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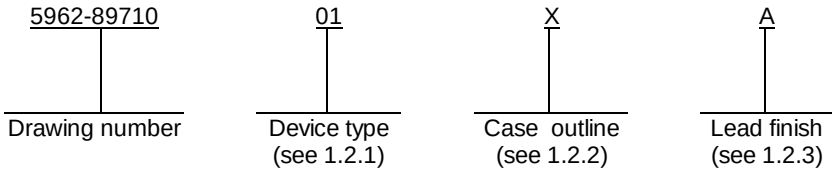
REV																				
SHEET																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C	C		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A	PREPARED BY Rick C. Officer	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles E. Besore	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, LINEAR, CMOS LATCHED 8- AND 16-CHANNEL ANALOG MULTIPLEXERS, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 90-08-08	
	REVISION LEVEL C	SIZE A CAGE CODE **67268** **5962-89710** SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADG526A	CMOS 16-channel multiplexer latched
02	ADG527A	CMOS 8-channel multiplexer latched

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (V_{DD}) to V_{SS} ..... 44 V dc
Supply voltage (V_{DD}) to GND ..... 25 V dc
V_{SS} to GND ..... -25 V dc
Analog inputs: 1/
  Voltage at S or D ..... V_{SS} –2.0 V dc to V_{DD} +2.0 V dc or 20 mA, whichever occurs first
  Continuous current, S or D ..... 20 mA
  Pulsed current, S or D (1.0 ms duration, 10% duty cycle) ..... 40 mA
DC input voltages 1/ ..... V_{SS} –4.0 V dc to V_{DD} +4.0 V dc or 20 mA, whichever occurs first
Storage temperature range ..... -65°C to +125°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Power dissipation to +75°C (P_D) ..... 470 mW 2/
Thermal resistance, junction-to-case (θ_{JC}):
  Cases X and 3 ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage to ground (V_{SS}) ..... -15 V dc
Supply voltage to ground (V_{DD}) ..... +15 V dc
Ambient operating temperature range ..... -55°C to +125°C

1/ Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, S, or D will be clamped by diodes. Current should be limited to the maximum rating above.
2/ Derate above T_A = +75°C at 6.0 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dual supply							
Analog signal range	V_{ANALOG}	$T_A = +25°C$ 2/	4	01, 02	-15	+15	V
Drain-source "ON" resistance	$R_{DS(ON)}$	$V_{DD} = 14.25$ V, $V_{SS} = -14.25$ V,	1	01, 02		300	Ω
		$I_{DS} = 1.0$ mA, $V_D = 5.0$ V, $V_S = V_D + (I_{DS} \times R_{ON})$	2, 3			400	
		$V_{DD} = 10.8$ V, $V_{SS} = -10.8$ V,	1			450	
		$I_{DS} = 1.0$ mA, $V_D = 5.0$ V, $V_S = V_D + (I_{DS} \times R_{ON})$	2, 3			600	
Source "OFF" leakage current	$I_{S(OFF)}$	3/	1	01, 02		1.0	nA
			2, 3			50	
Drain "OFF" leakage current	$I_{D(OFF)}$	3/	1	01		1.0	nA
			2, 3			200	
			1	02		1.0	
			2, 3			100	
Drain "ON" leakage current	$I_{D(ON)}$	3/	1	01		1.0	nA
			2, 3			200	
			1	02		1.0	
			2, 3			100	
Differential "OFF" output leakage current	$I_{DIFF(OFF)}$	3/	2, 3	02		25	nA
High level input current	I_{INH}	$V_{DD} = 16.5$V, $V_{SS} = -16.5$ V, $V_{IN} = 16.5$ V	1, 2, 3	01, 02		1.0	µA
Low level input current	I_{INL}	$V_{DD} = 16.5$V, $V_{SS} = -16.5$ V, $V_{IN} = 0$ V	1, 2, 3	01, 02		1.0	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dual supply - continued							
Supply current	I_{DD}	V_{DD} = 16.5 V, V_{SS} = -16.5 V V_{INH} = 2.4/15 V, V_{INL} = 0.8/0 V	1, 2, 3	01, 02		1.5	mA
Supply current	I_{SS}	V_{DD} = 16.5 V, V_{SS} = -16.5 V V_{INH} = 2.4/15 V, V_{INL} = 0.8/0 V	1, 2, 3	01, 02		0.2	mA
Delay time	t_{OPEN}	V_1 = ±10 V, See figure 3 4/	9	01, 02	25		ns
			10, 11		10		
Enable delay time	$t_{ON/OFF}$ (EN)	See figure 3 4/	9	01, 02		300	ns
			10, 11			400	
Single supply							
Analog signal range	V_{ANALOG}	T_A = +25°C, V_{SS} = 0 V 2/	4	01, 02	0	+15	V
Drain-source "ON" resistance	$R_{DS(ON)}$	V_{DD} = 10.8 V, V_{SS} = 0 V, I_{DS} = 0.5 mA, V_D = 5.0 V, $V_S = V_D + (I_{DS} \times R_{ON})$	1	01, 02		700	Ω
			2, 3			1000	
Source "OFF" leakage current	$I_{S(OFF)}$	5/	1	01, 02		1.0	nA
			2, 3			50	
Drain "OFF" leakage current	$I_{D(OFF)}$	5/	1	01		1.0	nA
			2, 3			200	
			1	02		1.0	
			2, 3			100	
Drain "ON" leakage current	$I_{D(ON)}$	5/	1	01		1.0	nA
			2, 3			200	
			1	02		1.0	
			2, 3			100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Single supply - continued							
Differential "OFF" output leakage current	$I_{DIFF(OFF)}$	5/	2, 3	02		25	nA
High level input current	I_{INH}	V_{DD} = 16.5V, V_{SS} = 0 V, V_{IN} = 16.5 V	1, 2, 3	01, 02		1.0	µA
Low level input current	I_{INL}	V_{DD} = 16.5V, V_{SS} = 0 V, V_{IN} = 0 V	1, 2, 3	01, 02		1.0	µA
Supply current	I_{DD}	V_{DD} = 16.5 V, V_{SS} = 0 V, V_{INH} = 2.4/15 V, V_{INL} = 0.8/0 V	1, 2, 3	01, 02		1.5	mA
Delay time	t_{OPEN}	V_1 = 10/0 V, V_{SS} = 0 V, See figure 3	9	01, 02	25		ns
		4/	10, 11		10		
Enable delay time	$t_{ON/OFF (EN)}$	V_{SS} = 0 V, See figure 3	9	01, 02		450	ns
		4/	10, 11			600	

1/ Unless otherwise specified, V_{DD} = +15 V, V_{SS} = -15 V and logic inputs are at desired logic levels (2.4 V and 0.8 V).

2/ This parameter is tested initially and after any process changes which may affect it.

3/ V_{DD} = +16.5 V, V_{SS} = -16.5 V, V_D = +10 V/ -10 V, V_S = -10 V/ +10 V, V_{INL} = 0.8 V, V_{INH} = 2.4 V.

4/ Figure 3 refers to device type 01. For device type 02 the test circuits are functionally identical, but there are some DUT pin name changes

5/ V_{DD} = +16.5 V, V_{SS} = 0 V, V_D = +10 V/ -10 V, V_S = 0 V/ +10 V, V_{INL} = 0.8 V, V_{INH} = 2.4 V.

Device types	01	02
Case outlines	X and 3	X and 3
Terminal number	Terminal symbol	
1	V_{DD}	V_{DD}
2	NC	DB
3	$\overline{RS}$	$\overline{RS}$
4	S16	S8B
5	S15	S7B
6	S14	S6B
7	S13	S5B
8	S12	S4B
9	S11	S3B
10	S10	S2B
11	S9	S1B
12	GND	GND
13	$\overline{WR}$	$\overline{WR}$
14	A3	NC
15	A2	A2
16	A1	A1
17	A0	A0
18	EN	EN
19	S1	S1A
20	S2	S2A
21	S3	S3A
22	S4	S4A
23	S5	S5A
24	S6	S6A
25	S7	S7A
26	S8	S8A
27	V_{SS}	V_{SS}
28	D	DA

NC = No connection

FIGURE 1. Terminal connections.

Device type 01

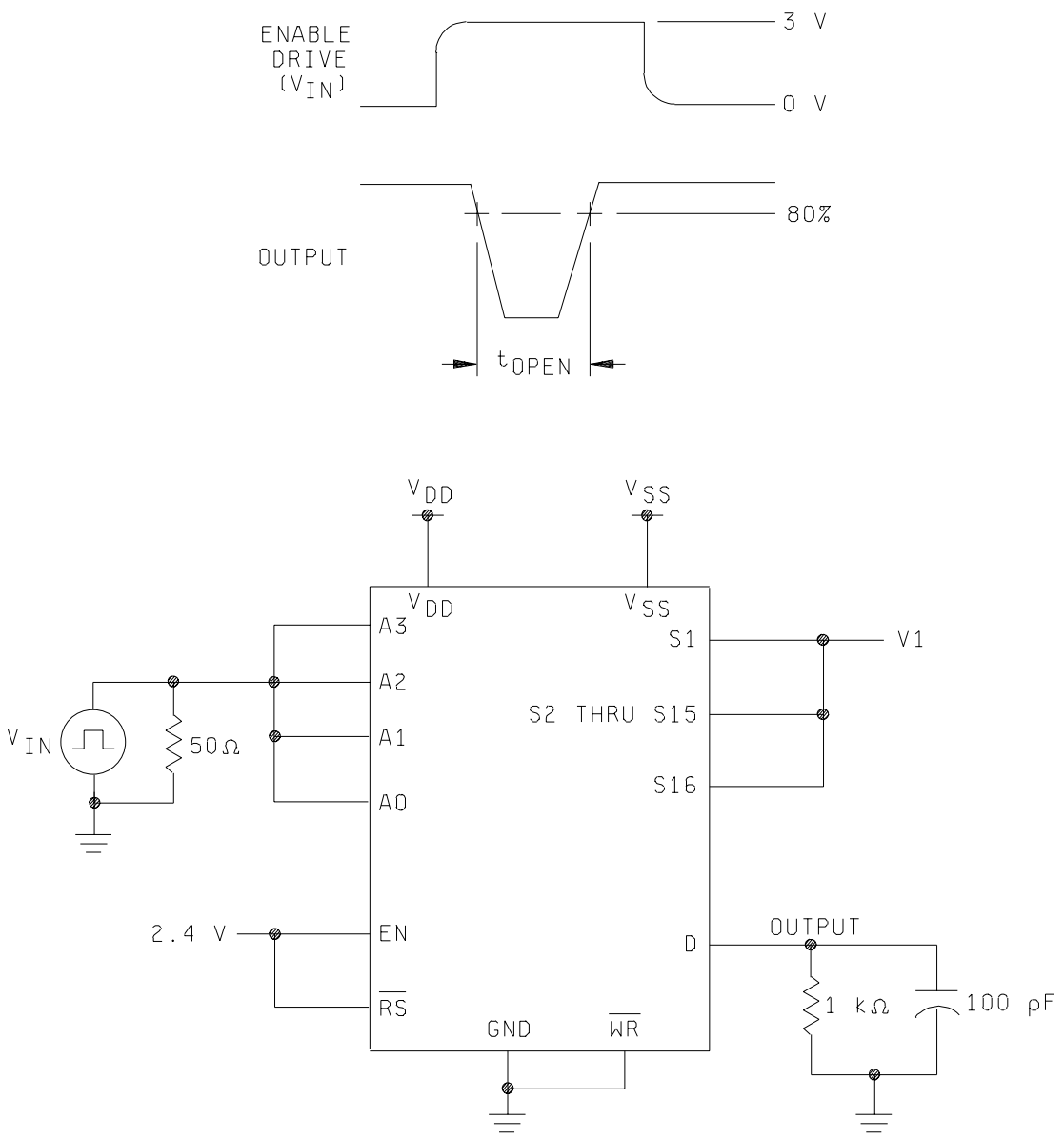
A3	A2	A1	A0	EN	$\overline{WR}$	RS	ON SWITCH
X	X	X	X	X	_┌¯	1	Retains previous switch condition
X	X	X	X	X	X	0	None (address and enable latches cleared)
X	X	X	X	0	0	1	None
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

Device type 02

A2	A1	A0	EN	$\overline{WR}$	RS	ON SWITCH
X	X	X	X	_┌¯	1	Retains previous switch condition
X	X	X	X	X	0	None (address and enable latches cleared)
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Do not care
_┌¯ = Signal is switching from low to high

FIGURE 2. Truth tables.



BREAK-BRFORE-MAKE DELAY, t_{OPEN}

FIGURE 3. Test circuits.

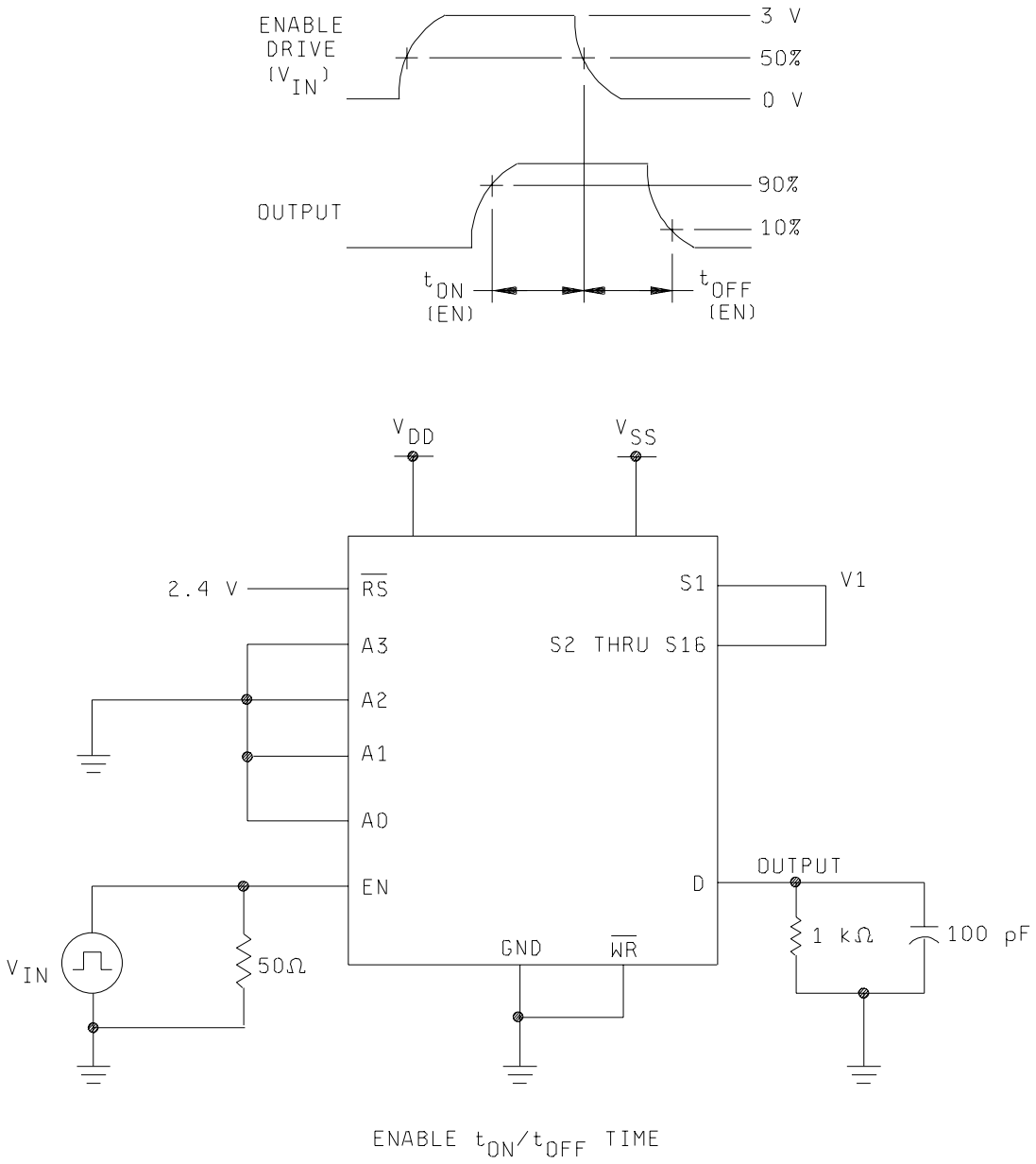


FIGURE 3. Test circuits - continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (analog signal range) shall be measured only for the initial test and after process or design changes which may affect analog signal range.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-09-14

Approved sources of supply for SMD 5962-89710 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-89710013A	24355	ADG526ATE/883B
5962-8971001XA	24355	ADG526ATQ/883B
5962-89710023A	24355	ADG527ATE/883B
5962-8971002XA	24355	ADG527ATQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland